Patent claims

1. Process for etching at least one substrate (10), in particular at least one silicon wafer for the fabrication of DRAM memory chips, in which

a) at least one substrate (10), for a first etching step (1), is arranged for a predetermined time in a first vessel containing a first etchant, then

b) at least one substrate (10), for a first rinsing step (2), is arranged for a predetermined time in a second vessel containing a first rinsing agent, the first rinsing agent containing at least one wetting agent, and then

c) at least one substrate (10), for a second etching step (3), is arranged for a predetermined time in a third vessel containing a second etchant.

2. Process according to Claim 1, characterized in that for at least one substrate (10), after the second etching step (3), a second rinsing step is carried out using a second rinsing agent in a fourth vessel.

3. Process according to Claim 2, characterized in that for at least one substrate (10) a drying step (5) is carried out after the second rinsing step (3).

4. Process according to Claim 1, characterized in that the first etchant includes a hydrofluoric acid fraction.

5. Process according to Claim 1, characterized in that the second etchant includes an ammonia water (NH_4OH) fraction.

6. Process according to Claim 5, characterized in that the first rinsing agent contains the wetting agent

in a concentration in the range from 0.01 to 0.1% by weight.

7. Process according to Claim 1, characterized in that in the second etching step (3) at least one structure (11) with an aspect ratio in the range from 10 to 50 is introduced into the substrate (10).

8. Process according to Claim 7, characterized in that the structure (11) is at least one deep trench structure for a DRAM memory cell.